AUTHORIZATION CONTROL CIRCUIT AND METHOD

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of electronic devices, and more particularly to an authorization control circuit and method.

BACKGROUND OF THE INVENTION

Electronic devices may need to control or disable various outputs in accordance with authorization information. Digital devices typically manipulate their own digital data output to a device that provides analog output to control or disable that analog output. Manipulating the digital data to disable the analog output can result in unwanted output artifacts. It also continues to require power for the conversion of digital data and the output of analog data. In addition, if the device receives power from a battery, that unnecessary power usage can shorten battery life.

SUMMARY OF THE INVENTION

Accordingly, a need has arisen in the art for an improved authorization control circuit. The present invention provides an authorization control circuit and method that substantially reduce or eliminate problems associated with prior authorization control systems.

In accordance with the present invention, an authorization control circuit comprises a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal. A digital to analog converter is coupled to the digital signal processor and is operable to receive the digital data output. The digital to analog converter generates analog data in response to the digital data output and is operable to output the analog data and mute the output of analog data. The digital to analog converter includes an input operable to receive the disable signal. The digital to analog converter mutes the output of analog data in response to the disable signal.

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More specifically, in accordance with one embodiment of the present invention, the authorization state is determined as either positive or negative. The digital signal processor is operable to generate the disable signal in response to a negative authorization state. The digital signal processor is operable to detect the disable signal and generate an override signal. The digital to analog converter is operable to cease muting the output of analog data in response to the override signal.

Technical advantages of the present invention include providing a authorization control circuit. In particular, the authorization control circuit may disable output from a digital source. Accordingly, power required to amplify the output is reduced. As a result, battery life may be increased. Another technical advantage is that output can be disabled without undesirable artifacts.

Other technical advantages of the present invention will be readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like parts, in which:

FIGURE 1 is a block diagram illustrating a system for playing digitally stored audio files in accordance with one embodiment of the present invention;

FIGURE 2 is a block diagram illustrating one embodiment of the present invention;

FIGURE 3 is a block diagram illustrating one embodiment of the present invention;

FIGURE 4 is a signal diagram illustrating the input format of digital data in accordance with one embodiment of the present invention; and

FIGURE 5 is a signal diagram illustrating the input format of control signals in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiments of the present invention and its advantages are best understood by referring now in more detail to the figures in which like numerals refer to like parts. FIGURE 1 illustrates a system for playing digitally stored audio files in accordance with one embodiment of the present invention. As described in more detail below, the system may include software for determining an authorization state. A disable signal may be generated if the authorization state is negative. A disable signal may also be generated when a sleep definition is met. An input in the signal processing circuits may control a muting function operable to receive the disable signal. Accordingly, unauthorized output can be prevented and power use can be reduced.

FIGURE 1 is a block diagram illustrating a system for playing digitally stored audio files including an authorization control circuit 10 for communicating data in an electronic device. The electronic device may also comprise a music, video, or multimedia file player or any other type of device that displays data to be heard or seen by the user.

Referring to FIGURE 1, the authorization control circuit 10 comprises a data storage 14 and a digital signal processor 12. In one embodiment, the digital signal processor can be a fixed-point digital signal processor made by Texas Instruments. In another embodiment, the digital signal processor could be a general purpose processor. Data files received from the storage 14 are processed in the digital signal processor 12.

In one embodiment, a file selected by the user to be played is first hashed by the digital signal processor 12. Hashing is running the file through a mathematical algorithm that yields a fixed-length value or key that represents the original file. The mathematical algorithm is the hashing function. A hashing function is secure if it is computationally infeasible to find a file that corresponds to a given value or key, or to find two different files which produce the same value or key. For example, the Secure Hashing Algorithm (SHA-1) was made available by the National Institute of Standards and Technology on April 17, 1995. By transforming a file with a secure hashing function and checking the key for the authorized file, the digital signal processor 12 can determine if the file has been changed (for example, illegally copied). An authorization state is determined by the comparison of the hashing result and the expected key. If they match, the authorization state is positive. If they do not, it is negative.

The digital signal processor 12, in one embodiment, can be programmed with a sleep function. The sleep function would monitor usage of the device and generate a sleep signal if usage meets predetermined criteria. For example, the criteria could be unchanged, repeat

play of a file for a certain period. In one embodiment, the sleep function could also allow for user customization of the time period criterion.

The digital signal processor 12 includes a digital data output 16, a bit clock output 18, and a channel output 20. Each output is connected to an input of a digital audio converter (DAC) 28. In one embodiment, the DAC 28 is a Codec. The DAC 28 reads digital data by sampling the digital data output 16 in accordance with the clock signal received from the bit clock output 18. If the DAC is operable to produce stereo output, it classifies the digital data as corresponding to the left or right analog channel by the state of the channel output 20 when the digital data is received.

FIGURE 4 illustrates a signal diagram of outputs 16,18,20. In one embodiment, digital bit 62 is read at the rising edge of bit clock output 18. The bit 62 corresponds to the analog channel indicated by the high state of channel output 20. The DAC receives a series of bits in one channel and then a series of bits in the other. In another embodiment, each bit could correspond to a different channel than the previous bit if the channel output 20 changed between each bit.

Referring to FIGURE 1, the DAC 28 converts the digital data to two channels of analog data 30,32. The analog data is transmitted to an amplifier 50 through coupling capacitors 34,36. The amplification of the first channel 30 is determined by the resistors 38,44. The amplification of the second channel 32 is determined by resistors 40, 48. Capacitors 42,46 can be included in parallel with the bypass resistors 44,48.

The two channels of amplified analog data are transmitted to output 56 via coupling capacitors 52,54. In one embodiment the output 56 is a pair of headphone speakers. The output could also be larger speakers or a video display, among other devices.

The digital signal processor also includes outputs separate from the data outputs 16,18,20 that control the muting function of the DAC 28. Those outputs are the mode word output 22, the mode bit output 24, and the mode data output 26. The DAC receives those outputs at mode inputs 23,25,27 which are operable to receive a mute signal.

FIGURE 5 illustrates a signal diagram of outputs 22,24,26. The mode word output 22 toggles to indicate the border between words (a sequence of a predetermined number of bits). The mode bit output 24 toggles to indicates the location of bits in the mode data 26. The mode data 26 includes address bits 64 that indicate which mode address is being modified by the word. The mode data 26 also includes function bits 66 and mute bit 68. The mute bit 68 is a signal that, when properly indicated by mode word and mode bit outputs 22,24, disables the analog

output by activating the DAC mute. The DAC mute can operate through a digital filter in the DAC which processes the digital data before it is converted into analog data.

The disable signal can be sent in response to a negative authorization state, a sleep signal, or other signals produced by the digital signal processor 12. For example, override software, placed on the digital signal processor 12 for testing or other reasons, can block the disable signal even though a negative authorization state has resulting from a hashing function-key comparison.

FIGURE 2 is a block diagram illustrating an embodiment of the present invention. In that embodiment, a DAC 60 with a single mute input 59 is included in authorization circuit 10. An output 58 on the digital signal processor 12 controls the mute function of the DAC 60 with a high or low signal. The DAC 60 receives digital data from outputs 16,18,20 and transmits analog data on two channels 30,32 as described with reference to FIGURE 1.

FIGURE 3 is a block diagram illustrating an embodiment of the present invention. In that embodiment, the single mute output 58 of the digital signal processor 12 is connected to an input 51 of amplifier 50 and controls the mute function of the amplifier 50 in response to an authorization state or sleep signal as discussed in reference to FIGURE 1. DAC 60 receives digital data from outputs 16,18,20 and transmits analog data on two channels 30,32 as described with reference to FIGURE 1. Amplifier 50 amplifies the analog data unless the mute function is selected by the disable signal in which case the analog data is muted.

Although the present invention has been described with several embodiments, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.